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Exercise Sheet 4

Computer Engineering and Communication Networks

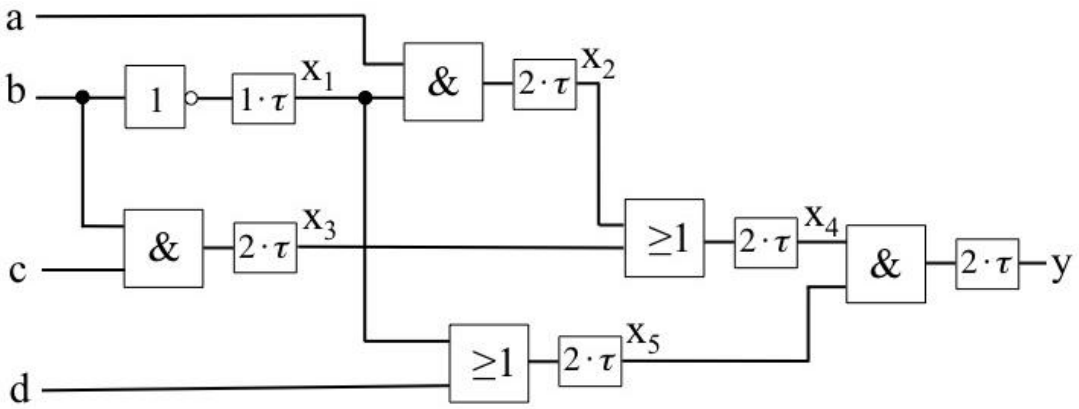
Handout: 11.10.2019
Discussion: 24.10.2019 (start 10:00 a.m.)

1. Combinatorial Circuits

1.1. Given the circuit diagram below and the delay (τ) for each gate, answer Question 1.1.1 and Question 1.1.2.

1.1.1. Complete the time diagram below.

1.1.2. Does a hazard error occur at exit y?



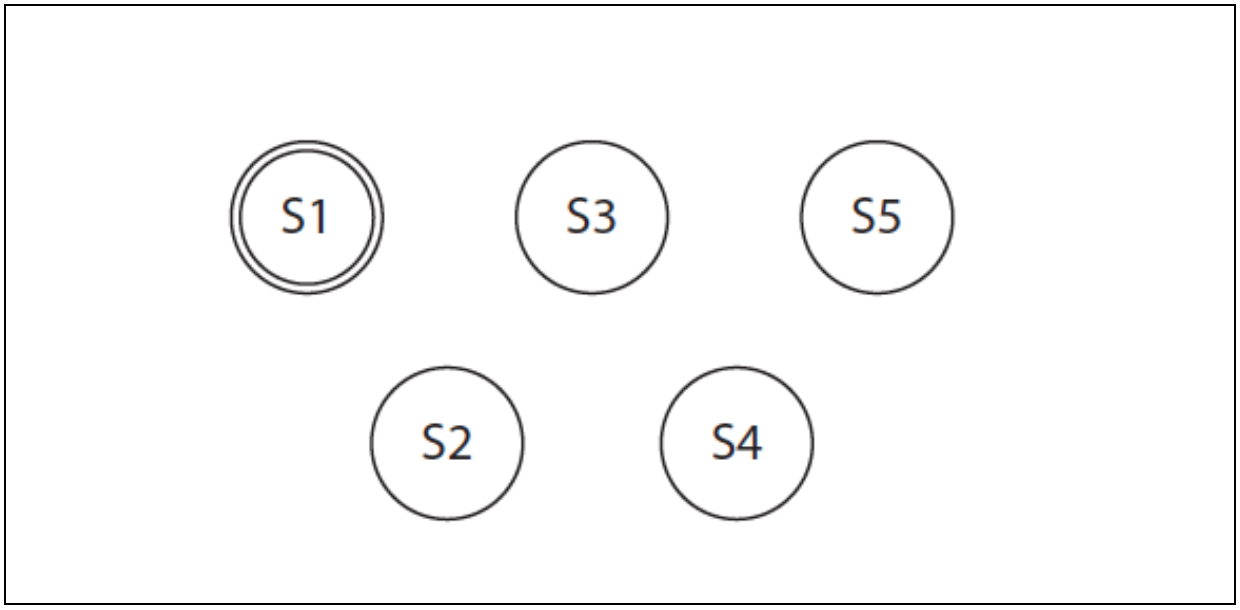
a	1 0										
b	1 0										
c	1 0										
d	1 0										
x_1	1 0										
x_2	1 0										

x_3	1 0										
x_4	1 0										
x_5	1 0										
y	1 0										
		$1\cdot\tau$	$2\cdot\tau$	$3\cdot\tau$	$4\cdot\tau$	$5\cdot\tau$	$6\cdot\tau$	$7\cdot\tau$	$8\cdot\tau$	$9\cdot\tau$	$10\cdot\tau$

2. Sequential Circuits

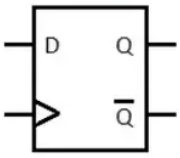
2.1. Model a Mealy-FSM that shows the following behavior:

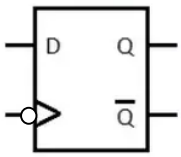
- As input only “a”, “b”, and “c” can be handled.
- As output only “0” or “1” can be produced.
- Before the sequence “abca” is given as input, the FSM produces all the time “0” as an output.
- After the sequence “abca” was given as an input, the FSM produces all the time “1” as an output.
- The states standing for the following:
  - S1 is the start state for the FSM
  - S2 equals “a”
  - S3 equals “ab”
  - S4 equals “abc”
  - S5 equals “abca”



2.2. What is the condition that must be always observed in an RS flipflop?

2.3. Which one of this two D Flipflops is triggered in the negative edge?

A) 

B) 

2.4. Which type of flipflop presents a control function to change stored value?

2.5. What is the Control Table for the following flipflops:

   2.5.1. RS Flipflop

   2.5.2. JK Flipflop