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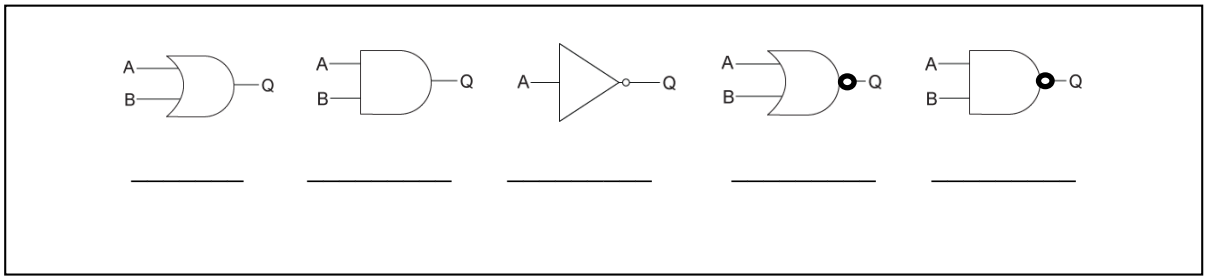
Exercise Sheet 3

Computer Engineering and Communication Networks

Handout: 11.10.2018
Discussion: 18.10.2018 (start 10:00 a.m.)

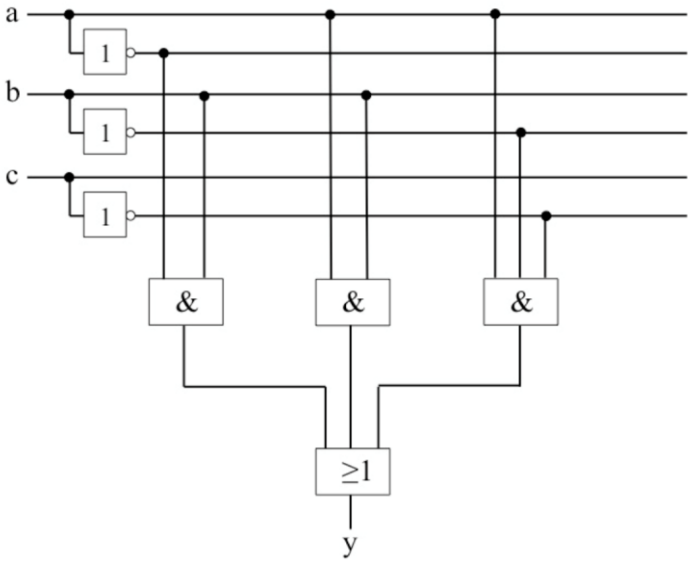
1. Name the following logic gates:



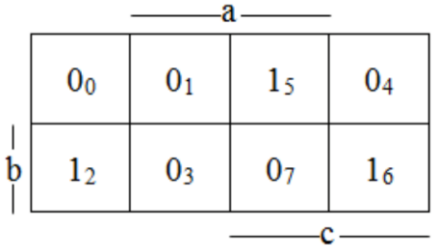
2. Design a logic circuit using the gates OR, AND, and NOT of the Boolean expression below:

$$((a \wedge \overline{a}) \wedge (a \vee \overline{b})) \vee (\overline{c} \wedge b \wedge a)$$

3. Given the block diagram below.
   3.1. Which Boolean expression is represented by this block diagram?
   3.2. Simplify the Boolean expression as far as possible using Boolean Algebra Instantiations.

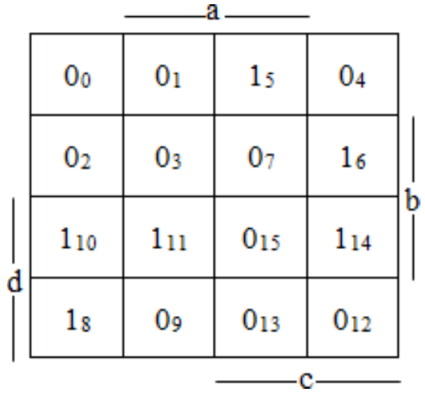


4. Given is the following KV-Diagram. State if the given statement is true or false and justify the answer.



1. Statement 1: The max term at index 4 equals the expression $\bar{a} \vee b \vee \bar{c}$.
2. Statement 2: Index 0 is the only index where all the minterm variables (a,b,c) are complemented.
3. Statement 3: Index 7 is the only index where all the maxterm variables (a,b,c) are not complemented.

5. Given the following KV-Diagram.



5.1 Determine the Minterms.
5.2 Determine all prime implicants.
5.3 Determine the minimal DNF.