Fall Term 2018, Department of Informatics IfI, UZH, Switzerland

Computer Engineering and Communication Networks (CECN)

Dr. Rehan Ahmed
Slides prepared by Prof. Dr. Burkhard Stiller
Communication Systems Group CSG
Department of Informatics IfI, University of Zürich UZH
Binzmühlestrasse 14, CH-8050 Zürich, Switzerland

Universität Zürich[UZH]

Phone: +41 44 632 70 41
E-Mail: rehan.ahmed@tik.ee.ethz.ch

CSG Communication Systems Group

Assistents:
Eder John Scheid, Sina Rafati
Phone: +41 44 635 [7585|7586], FAX: +41 44 635 6809
E-Mail: [scheid|rafati]@ifi.uzh.ch

Lecture Goals

- Computer Engineering
  - Competencies in basic systems of underlying hardware and computer architecture
  - To understand that solutions do almost always see a combination of hardware and software with many constraints: costs, temperature, performance ...
  - Basic concepts of information processing in digital forms (data, numbers, chars)
    - Boolean Logic
    - Gates, Arithmestic Logical Unit, and Central Processung Unit
    - Basics of chips and computer architecture (performance)
- Communication Networks
  - To understand key concepts of communication networks as ***the*** major pillar of today's society based on ICT (Information and Communications Technology)
  - To understand how the Internet and selected distributed applications work, the Internet being ***the*** prototype of today's as well as future communication and information networks.
  - To be able to extrapolate from today's network and systems examples to future research and development issues and topics.

Lecture Content (1)

- Basics and Introduction
- Arithmetics
  - Number systems, number representation
  - Basic aritrhmetic operations, characters
- Combinatorial Circuits
  - Formal basics of logic (Boolean Algebra), normal- and minimal forms
  - Implementation based on gates, design, and effects of transit times
- Sequential Circuits
  - Formal basics (Finite State Machine)
  - Asynchronous circuits and flipflops, synchronous and dedicated circuits
  - Arithmetic Logical Unit (ALU)
- Computer Architecture and Organization
  - von-Neumann architecture
  - Command formats, data types, addressing
  - Memory and caches
  - Organization in components busses, interfaces, peripherials
  - Technology development

Lecture Content (2)

- History of Communications
- Communication Architectures, Services, and Protocols
  - Communication Characteristics, Layering Examples
- Basic Concepts
  - Building blocks, point-to-point links, reliable service over unreliable channels
- Shared Direct Links (Broadcast)
  - Local Area Networks: Ethernet family, FDDI
- Packet Switching and Internetworking (Network Layer)
  - Internet Protocol and routing
- End-to-end Protocols (Transport Layer)
  - User Datagram Protocol (UDP), Transmission Control Protocol (TCP)
- Security Mechanisms and Protocols
- Applications and Mechanisms (Application Layer)
  - E-mail, Domain Name System (DNS), World Wide Web (WWW)
- Summary and Outlook

Organizational Issues

Teaching Material

- Lecture slides
  - http://www.csg.uzh.ch/teaching/hs17/cecn.html
  - Slides accessible ONLY with a UZH-internal IP address (VPN)
- Reading material
  - Text books (mandatory):
    - H. Herold, B. Lurz, J. Wohlrab: Grundlagen der Informatik, Pearson Studium, München, 2012, 2. Auflage, ISBN-13 978-3-86894-111-1 (in German)
    - https://en.wikiversity.org/wiki/Introduction_to_Computers (in English, covering parts of the Herold et al. book)
    - URLs: Karnaugh-Veitch-Diagramme http://ti.itec.uka.de/KVD/ (Universität Karlsruhe)
    - A. S. Tanenbaum, David J. Wetherall: C*omputer Networks;* 5th Edition, 2011 Prentice Hall, Indian International Ed, ISBN-13: 978-0-13-212695-3 (in English)

Contact Information

- Lecture: Thursdays 8.15am – 9.45am
  15 min break
  and 10.00am – 11.30am (partially)
- Exercises: Thursdays 10.00am – 11.30am (partially)

Room: 2.A.10

- Access to (additional) lecture information:
  http://www.csg.uzh.ch/teaching/hs18/cecn.html
- Lecturer contact:
  - Via email: rehan.ahmed@tik.ee.ethz.ch

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Lecture and Exercise Plan for HS17

Sept 20	2+2 h lecture
Sept 27	2 h lecture + 2 h exercise
Oct 4	2+2 h lecture
Oct 11	2 h lecture + 2 h exercise
Oct 18	2 h lecture +2 h exercise
Oct 25	2 h lecture + 2 h exercise
Nov 1	2 h lecture +2 h exercise
Nov 8	2 +2 h lecture
Nov 15	2 h lecture +2 h exercise
Nov 22	2 h lecture + 2 h exercise
Nov 29	2 h lecture +2 h exercise
Dec 6	2+2 h lecture
Dec 13	2 h lecture +2 h exercise
Dec 20	2 h lecture + 2 h exercise

— Computer Engineering —
Module 1: Basics and Introduction

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Current State of Affairs

- Computer-based devices daily activities:
  - Hand-held/wearable computer
- Computer become “invisible” and become available in vast quantities:
  - Intelligent clothing, Internet-of-Things (IoT), ubiquitous systems, integrated control

- Everything communicates with anything:
  - Radio networks, mobiles, Bluetooth, UMTS, fiber optics, WWW/ …
- Integrated circuits, chips, computer engineering, communication networks shape today’s and tomorrow’s economies and societies:
  - *E.g.,* boom and dead calm of hardware industry impacts politics
  - *E.g.*, Information and Communication Technology (ICT) is today’s society’s pillar

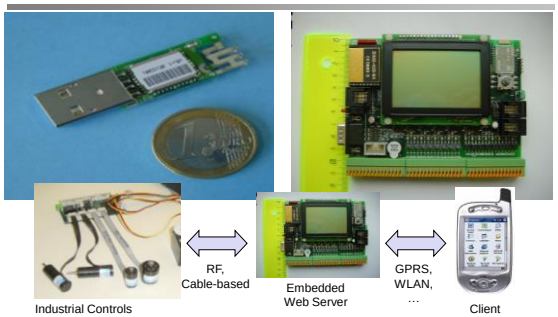
Example: Information Technology in Cars

- Emergency services
- Theft prevention
- Communications (e-mail, WWW, SMS, GSM, ...)
- Information services
- Remote diagnosis, remotre maintenance
- Navigation, routing (traffic)
- Engine control, ABS, ESP, ...

...or in a sweing machine!

Example: Communication Technology

Examples: Bluetooth Module, Web-Server, ...



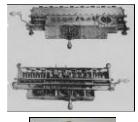
Developments in Computer Science

- Abakus a calculus board with marbles, typically wood or glas
  - Used more than 3000 years ago in China
  - Addition, subtraction, multiplication, and division
    - As well as extracting of square and cbic roots

- Algorithms
  - Persian mathematician and astronomer Ibn Musa Al-Chwarismi (9th century)
  - Processing rule, which humans as well as machines can perform
  - Precision needed besides oral languages to define rules uniquely (no interpretation)

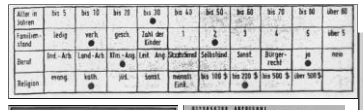
Steps from 1500 to 1930 (1)

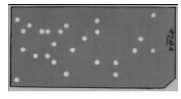
- Important steps:
  - A. Riese (1492-1559; Staffelstein) – Calculus rules for the decimal system
  - W. Schickard (1592-1635; Tübingen) – First computing device (Rechenmaschine)
  - B. Pascal (1623-1662; Clermont) – Computing device with 6 positions
  - G. Leibniz (1646-1716; Leipzig) – Machine for 4 basic arithmetics
  - P. Hahn (1739-1790; Kornwestheim) – 1st mechanical computing device

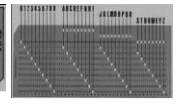


Steps from 1500 to 1930 (2)

- Charles Babbage (1792-1871) – Principle of the "Analytical Engine"
- Hermann Hollerith (1860-1929) – Inventor of the punch hole card

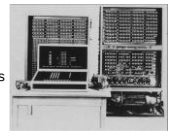






1st Operational Computer (1940's)

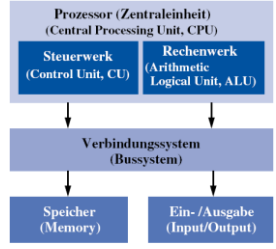
- Starting with electrical engineering advances electromechanical components appeared
  - Konrad Zuse built those in Berlin in 1941
  - The electromechanical Z3 used 2,600 air gap switches (Relais) and 64 memory positions with 22 Bit each
  - Multiplications worked in about 3 seconds



- Howard Aiken built in 1944 – in collaboration with Harvard University and IBM – the partially program-driven computing machinery Mark I.
  - Used about 100,000 parts
  - About 15 m long
  - Addition in about 1/3 second.
  - Multiplication in about 3 seconds.

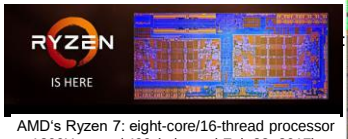
John von Neumann Architecture

- Mid 1940 John von Neumann developed the fundamental principles of a computer.
  - Central Processing Unit (CPU)
    - Control Unit
    - Arithmetic Logical Unit (ALU)
  - Bus system for interconnections
  - Memory for programs and data
  - Input/ouput interfaces/devices
  - Constrained jumps and branches

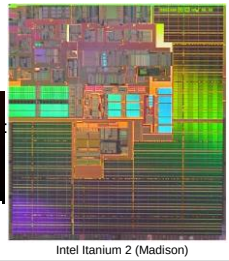


Micro Processors – The Formula 1 in CS

- "Das Wettrennen um die schnellsten Mikroprozessoren könnte man als Formel 1 der Computertechnik bezeichnen." (Die ZEIT vom 18. März 1994)
  - "The race for the fastest micro processors could be named as the formula 1 of computer science."



AMD's Ryzen 7: eight-core/16-thread processor 1800X costs $499 (released Feb 22, 2017)

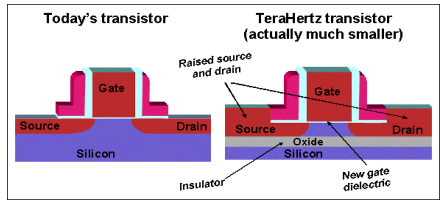


Intel Itanium 2 (Madison)

Example: Terahertz Transistor (Intel)

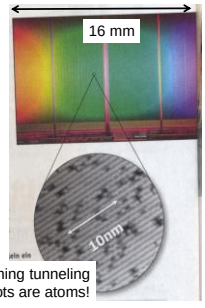
- Peak Transit Frequency: 2.63 THz, which equals a 0,38 ps gate delay!
  - Only at 0,000 000 000 000 38 s ...
  - Or less than 76 µm path for electromagnetic waves...

Tera: 10^{12}
pico: 10^{-12}
micro: 10^{-6}



Circuits, CPUs – At Scale

- 25 nm NAND memory chips
  - 8 GByte memory with 167 mm² surface area
  - Stackable – since 2010 done
- Intels XEON 5600 Series
  - 32 nm technology
  - Up to 6 Cores



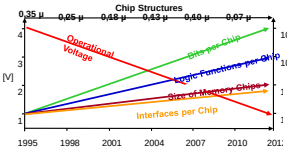
Picture of a scanning tunneling microscope: white dots are atoms!

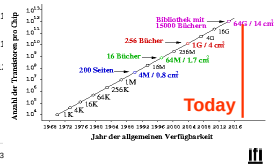
Moore's Law

- Number of transistors per (processor) chip doubles every 2 years.
- Computing power of high speed processors doubles every 18 months.
- At the same costs micro electronics delivers double the performance every 2 years.
- A chip manufacturing plant was the most expensinve single investment into a factory in 2002 (10 Billion US-Dollar).
- Only cooperations of larger companies will drive innovation:
  - EUVLLC (extrem ultraviolet limited liability company) from AMD, Motorola, Intel

Trends

- More transistors per chip
  - SIA Roadmap for technology trends
    - SIA = American Semiconductor Industry: http://public.itrs.net/
- Enhanced power at lower energy demand





- Memory size of memory chips